ARRANGEMENT COMPRISING A FIRST SEMICONDUCTOR CHIP AND A SECOND SEMICONDUCTOR CHIP CONNECTED THERETO

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ABSTRACT

An arrangement including a first semiconductor chip and a second semiconductor chip connected thereto, where the second semiconductor chip is additionally connected to electrical loads and drives these electrical loads on the basis of a timing which is prescribed to it by load control data, and where the first semiconductor chip transmits to the second semiconductor chip the aforementioned load control data and pilot data which control the second semiconductor chip, and where the second semiconductor chip transmits to the first semiconductor chip diagnostic data which represent states prevailing in the second semiconductor chip or events which occur. The diagnostic data are transmitted via a first transmission channel and the load control data and the pilot data are transmitted via a second transmission channel.